IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Yang, et al.**	Art Unit: 2814
Serial No.: 10/618,156	Examiner: Trinh, Hoa B.
Filed: July 11, 2003	
For: **Memory Structure Having Tunable Interlayer Dielectric and Method for Fabricating Same**	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 1-11 and 22-29. The Final Rejection issued on May 2, 2005. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on August 1, 2005.

REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

STATUS OF CLAIMS

Claims 1-11 and 22-29 are pending, and claims 12-21 were canceled in previous amendments. Claims 1-11 and 22-29 have been finally rejected in a Final Rejection dated May 2, 2005. This Appeal is directed to the rejection of claims 1-11 and 22-29, which appear in the attached "Appendix of Claims on Appeal."

STATUS OF AMENDMENTS

No claim amendments have been submitted in response to or subsequent to the Final Rejection dated May 2, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

A. Claim 1

Independent claim 1 defines a memory transistor structure (e.g., structure 100 in Figure 1A) comprising a substrate (e.g., substrate 102 in Figure 1A) and a channel region (e.g., channel region 108 in Figure 1A) that is situated between a drain region (e.g., drain

region 104 in Figure 1A), and a source region (e.g., source region 106 in Figure 1A). The memory transistor includes a gate layer (e.g., gate stack 110 including floating gate dielectric layer 111 in Figure 1A). *See*, e.g., page 7, lines 9-11 of the present application. The gate layer is situated over the channel region.

Independent claim 1 defines an invention which utilizes a tunable interlayer dielectric (e.g., tunable interlayer dielectric 114 in Figure 1A, or tunable interlayer dielectric 200 in Figure 2, or tunable interlayer dielectric 300 in Figure 3) formed over the gate layer and the substrate. The tunable interlayer dielectric includes a matrix and tunable material situated with the matrix (e.g., polymer matrix 202 in Figure 2 having liquid crystal droplets 204a, 204b and 204c or polymer matrix 302 in Figure 3 having liquid crystal droplets 304a, 304b and 304c). The tunable interlayer dielectric has a transparent state (as shown in Figure 1A and Figure 3) and an opaque state (as shown in Figure 1B and Figure 2). *See*, e.g., page 9 line 16 through page 10, line 6; *See* also, page 8, line 10 through page 9, line 2; and page 9 lines 4 to 15. The transparent state allows ultraviolet (UV) rays to pass through to the gate layer while the opaque state prevents UV rays to pass through to the gate layer.

B. Claim 22

Independent claim 22 defines substantially the same subject matter as independent claim 1.

GROUND(S) OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-11 and 22-29 under 35 USC § 103(a) as being unpatentable over U.S. Patent No. 5,999,152 to Liao et al. (hereinafter "Liao") in view of U.S. Patent No. 6,545,739 to Matsumoto et al. (hereinafter "Matsumoto").

ARGUMENT

The Examiner has rejected claims 1-11 and 22-29 under 35 USC § 103(a) as being unpatentable over Liao in view of Matsumoto. For the reasons discussed below, Applicant submits that:

(1) The finality of the rejection over Matsumoto was improper (i.e. a Non-Final Office Action should have issued, not a Final Office Action); and

(2) Even if the Final Office Action were properly issued, the present invention, as defined by independent claims 1 and 22, is patentably distinguishable over Liao in view of Matsumoto.

1. The finality of the rejection over Matsumoto was improper (i.e. a Non-Final Office Action should have issued, not a Final Office Action)

In the Office Action dated May 2, 2005, the Examiner has *finally rejected* claims 1-11 and 22-29 pending in the application on the basis of *new ground(s)* of rejection and newly cited art. Applicant respectfully requests reconsideration and withdrawal of the finality of the rejection of

the Office Action dated May 2, 2005, so that Applicant might have a meaningful opportunity to present new arguments and, if deemed appropriate, amend the pending claims (both for the purpose of examination by the Examiner, and for the purpose of a potential later appeal). The new reference is U.S. Patent No. 6,545,739 to Matsumoto, et al., which was for the first time brought to Applicant's attention by means of the *final rejection* dated May 2, 2005. The new reference, i.e. Matsumoto, was not cited in the present application prior to the final rejection of May 2, 2005.

It is noted that on page 4, paragraph 5 of the Final Office Action of May 2, 2005, the Examiner has stated that "Applicant's amendment necessitated the new ground(s) of rejection." However, Applicant's previous amendment merely changed the term "structure" to "transistor." In contrast, Matsumoto has been cited by the Examiner to support the Examiner's proposition that a "tunable dielectric layer" as disclosed and claimed in the present application is taught by Matsumoto, while the Examiner acknowledges that the "tunable dielectric layer" was not disclosed or suggested by the previously cited reference U.S. Patent No. 5,999,152 to Liao, et al. *See* Final Office Action of May 2, 2005, page 2, last two lines, and page 3, last three lines of the first paragraph.

Applicant submits that the limitation of a "tunable dielectric" was expressly claimed even prior to the Applicant's amendment and response to the Non-Final Office Action and that Applicant's amendment and response to the Non-Final Office Action (i.e. the changing of the term "structure" to "transistor") did not in any way necessitate citation and reliance on

Matsumoto - which the Examiner has cited in relation to the "tunable dielectric" limitation that appeared in the original unamended claims.

Since Matsumoto is a reference upon which the Examiner has relied for the first time through the Final Office Action of May 2, 2005, Applicant submits that it would be manifestly unfair for the Patent Office not to provide Applicant with a meaningful chance to amend the pending claims, if deemed appropriate, and/or to present new arguments necessitated due to the newly cited reference, Matsumoto. As such, a good and sufficient reason exists, as required by 37 CFR §1.116(c), for withdrawing the finality of the Office Action of May 2, 2005, and requesting that the Examiner issue the Office Action of May 2, 2005 as a Non-Final Office Action.

2. Even if the Final Office Action were properly issued, the present invention, as defined by independent claims 1 and 22, is patentably distinguishable over Liao in view of Matsumoto

Liao is directed to an electro-optic display providing a gray scale by utilizing voltage dependent birefringence. A voltage provided to metal pad "d" in Figure 1 of Liao is controlled through the gate voltage at "c" and the bit line voltage at source "b" of a MOS transistor. Each such MOS transistor and its corresponding metal pad "d" corresponds to a pixel. Based on the voltage provided to metal pad "d," the polarization of light passing through liquid crystal molecules "i" in Figure 2 of Liao is controlled such that light can be reflected back to the light source or be reflected to a viewer's eyes. *See*

Figures 3 and 4 of Liao and column 5, lines 14 to 45 of Liao. However, Liao is not directed to utilization and control of a tunable interlayer dielectric having a matrix including a tunable material capable of being "tuned to" a UV transparent or opaque state, as disclosed and claimed by the present invention.

Thus, Liao does not disclose or suggest accommodation of erasing stored charges in a gate layer, such as a gate layer of a flash memory transistor, when the matrix comprising tunable material is turned into a UV transparent state. *See*, for example, Figure 1A and page 11, lines 16-19, discussing step 408 of flow chart 400 in the present application. Nor does Liao disclose or suggest prevention of undesirable charge storage or blocking damage to a memory transistor needing protection from UV radiation, when the matrix comprising tunable material is turned into a UV opaque state. *See*, for example, Figure 1B and page 12, lines 3-6, discussing step 410 of flow chart 400 in the present application. Thus, the presently claimed invention is patentably distinguishable over Liao.

In the Final Office Action, the Examiner has acknowledged that Liao "does not explicitly teach that the dielectric is a tunable interlayer dielectric." The Final Office Action of May 2, 2005, page 2, last two lines. However, the Examiner has newly cited, and relied for the first time on, Matsumoto as overcoming this significant deficiency of Liao. Applicant submits that Matsumoto also fails to disclose or suggest "a tunable interlayer dielectric formed over said gate layer and said substrate, said tunable interlayer dielectric comprising a matrix and tunable material situated within said matrix, said

tunable interlayer dielectric having a transparent state and an opaque state, said transparent state allowing UV rays to pass through said tunable interlayer dielectric to said gate layer, said opaque state preventing UV rays to pass through said tunable interlayer dielectric to said gate layer," as disclosed and claimed in the present application.

Matsumoto is directed to a "Fabry-Perot etalon type" tunable wavelength-selective filter having two layers of transparent electrodes and optical mirrors flanking an intermediate layer of material with a refractive index that is variable with electric field, the intermediate layer is fabricated by dispersing liquid crystal droplets in a light transmissive medium such as a polymer or silica glass, and by adding plasticizer. *See*, e.g., Figures 1, 2A and 2B of Matsumoto, and column 6, lines 1-67. However, Matsumoto is directed to a filter utilized in wavelength-division multiplexing in optical communications, where different wavelengths of optical pulses traversing through optical fibers need be distinguished. *See*, e.g., column 1 lines 19-31 and column 2, lines 48-63 of Matsumoto.

As such, Matsumoto is not directed to "a tunable interlayer dielectric formed over said gate layer and said substrate, said tunable interlayer dielectric comprising a matrix and tunable material situated within said matrix, said tunable interlayer dielectric having a transparent state and an opaque state, said transparent state allowing UV rays to pass through said tunable interlayer dielectric to said gate layer, said opaque state preventing UV rays to pass through said tunable interlayer dielectric to said gate layer," as disclosed

and claimed in the present application. In other words, Matsumoto is not directed to use of a tunable interlayer dielectric, nor is Matsumoto directed to use of such dielectric to block or pass through UV rays. Moreover, Matsumoto is not directed to use of such dielectric in a memory transistor to prevent the transistor gate from storing unwanted charges as a result of unwanted UV rays during fabrication. *See*, for example, Figure 1B and page 12, lines 3-6, discussing step 410 of flow chart 400 in the present application. Further, Matsumoto is not directed to use of such dielectric in a memory transistor to accommodate the erasing of unwanted process induced charges by employing UV rays. *See*, for example, Figure 1A and page 11, lines 16-19, discussing step 408 of flow chart 400 in the present application. Moreover, there is no suggestion in either Matsumoto or Liao, and the Examiner has not pointed to any purported suggestion, to combine Liao with Matsumoto in order to achieve the present invention as defined by independent claims 11 and 22.

CONCLUSION

As discussed above, Applicant respectfully requests withdrawal of the finality of the Office Action of May 2, 2005 since a new reference, Matsumoto, was cited and relied upon for the first time in that Office Action. In any event, for all the foregoing reasons, Applicant respectfully submits that pending claims 1-11 and 22-29 are patentably distinguishable over Liao and Matsumoto, either singly or in combination. Thus, an early

notice of allowance directed to claims 1-11 and 22-29 remaining in the present application is respectfully requested.

This Appeal Brief is submitted herewith with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 10/28/05

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Date of Deposit: 10/28/05

Christina Carter
Name of Person Mailing Paper and/or Fee

Christina Carter 10/28/05
Signature Date

APPENDIX OF CLAIMS ON APPEAL

Claim 1: A memory transistor comprising:

a substrate having a drain region, a source region and a channel region, said channel region being between said source region and said drain region;

a gate layer formed over said channel region of said substrate;

a tunable interlayer dielectric formed over said gate layer and said substrate, said tunable interlayer dielectric comprising a matrix and tunable material situated within said matrix, said tunable interlayer dielectric having a transparent state and an opaque state, said transparent state allowing UV rays to pass through said tunable interlayer dielectric to said gate layer, said opaque state preventing UV rays to pass through said tunable interlayer dielectric to said gate layer.

Claim 2: The memory transistor of claim 1, wherein said tunable material comprises a plurality of liquid crystal droplets, each of said plurality of liquid crystal droplets having a corresponding crystal director, said corresponding crystal director defining a polar orientation of each of said plurality of liquid crystal droplets.

Claim 3: The memory transistor of claim 2, wherein said corresponding crystal director has a random orientation within said matrix during said opaque state.

Claim 4: The memory transistor of claim 3, wherein said opaque state is enabled when an electric field is not applied across said tunable interlayer dielectric.

Claim 5: The memory transistor of claim 3, wherein said opaque state is enabled when a magnetic field is applied across said tunable interlayer dielectric.

Claim 6: The memory transistor of claim 2, wherein said corresponding crystal director has a uniform orientation within said matrix during said transparent state.

Claim 7: The memory transistor of claim 6, wherein said transparent state is enabled when an electric field is applied across said tunable interlayer dielectric.

Claim 8: The memory transistor of claim 6, wherein said transparent state is enabled when a magnetic field is not applied across said tunable interlayer dielectric.

Claim 9: The memory transistor of claim 1, wherein said tunable material is selected from the group consisting of electrically tunable material and magnetically tunable material.

Claim 10: The memory transistor of claim 1, wherein said matrix is polymer.

Claim 11: The memory transistor of claim 1, wherein said gate layer includes a charge storing layer.

Claim 22: A memory transistor comprising a substrate having a drain region, a source region and a channel region, said channel region being between said source region and said drain region, said memory transistor further comprising a gate layer formed over said channel region of said substrate, said gate layer including a charge storing layer, said memory transistor characterized by:

a tunable interlayer dielectric formed over said gate layer and said substrate, said tunable interlayer dielectric comprising a matrix and tunable material situated within said matrix, said tunable interlayer dielectric having a transparent state and an opaque state, said transparent state allowing UV rays to pass through said tunable interlayer dielectric to said gate layer, said opaque state preventing UV rays from passing through said tunable interlayer dielectric to said gate layer.

Claim 23: The memory transistor of claim 22, wherein said tunable material comprises a plurality of liquid crystal droplets, each of said plurality of liquid crystal droplets having a corresponding crystal director, said corresponding crystal director defining a polar orientation of each of said plurality of liquid crystal droplets.

Claim 24: The memory transistor of claim 23, wherein, during said opaque state, said corresponding crystal director has a random orientation within said matrix.

Claim 25: The memory transistor of claim 23, wherein, during said transparent state, said corresponding crystal director has a uniform orientation within said matrix.

Claim 26: The memory transistor of claim 25, wherein said transparent state is enabled by providing an electric field through said tunable interlayer dielectric.

Claim 27: The memory transistor of claim 22, wherein said tunable material is selected from the group consisting of electrically tunable material and magnetically tunable material.

Claim 28: The memory transistor of claim 22, wherein said matrix is polymer.

Claim 29: The memory transistor of claim 22, wherein said gate layer includes a charge storing layer.

EVIDENCE APPENDIX

(NONE)

RELATED PROCEEDINGS APPENDIX

(NONE)